

HCT65N27M1

N-Channel eSiC Silicon Carbide Power MOSFET

650 V, 84 A, 27 mΩ

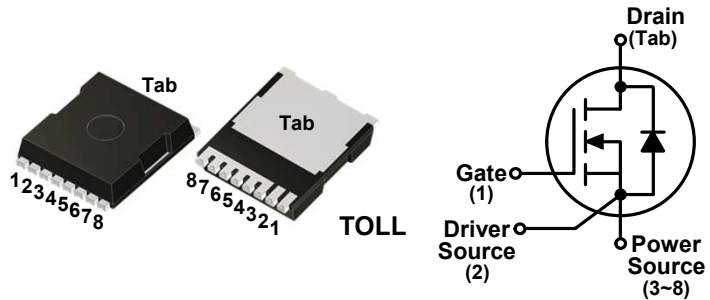
Features

- High switching speed with a low gate charge
- Fast intrinsic diode with low reverse recovery
- Robust Avalanche Capability
- 100% Avalanche Tested
- Pb-free, Halogen Free, and RoHS Compliant

$BV_{DSS}, T_C=25^{\circ}\text{C}$	$I_D, T_C=25^{\circ}\text{C}$	$R_{DS(on),typ}$	$Q_{g,typ}$
650 V	84 A	27 mΩ	91 nC

Benefits

- System efficiency improvement
- Higher frequency applicability
- Increased power density
- Reduced cooling effort



Applications

- Server & Telecom power
- EV charging station
- Solar inverter / ESS / UPS
- Industrial power supply



Absolute Maximum Ratings ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GS}	Gate to Source Voltage (DC)		-10 / +22	V
V_{GSop}	Recommended Operation Value		-5 / +18	V
I_D	Drain Current	Continuous ($T_C = 25^{\circ}\text{C}$)	84	A
		Continuous ($T_C = 100^{\circ}\text{C}$)	60	
I_{DM}	Drain Current	Pulsed (Note1)	225	A
P_D	Power Dissipation	($T_C = 25^{\circ}\text{C}$)	349	W
		Derate Above 25°C	2.33	W/ $^{\circ}\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 175	$^{\circ}\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		260	$^{\circ}\text{C}$

※Note 1 : Limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.43	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
HCT65N27M1	HCT65N27M1	TOLL	Tape & Reel	1000 units

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		1	100	μA
		$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$		10		
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = +22\text{ V}, V_{DS} = 0\text{ V}$			+100	nA
		$V_{GS} = -10\text{ V}, V_{DS} = 0\text{ V}$			-100	

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 11.7\text{ mA}$ (tested after $V_{GS} = 22\text{ V}, 1\text{ ms pulse}$)	1.8	2.8	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 18\text{ V}, I_D = 35\text{ A}$		27	38	m Ω
		$V_{GS} = 18\text{ V}, I_D = 35\text{ A}, T_J = 175^\circ\text{C}$		35		
g_{fs}	Transconductance	$V_{DS} = 20\text{ V}, I_D = 35\text{ A}$		25.9		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$		1853		pF
C_{oss}	Output Capacitance			207		
C_{rss}	Reverse Capacitance			10.5		
E_{oss}	Stored Energy in Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		20.6		μJ
$C_{o(er)}$	Energy Related Output Capacitance			257		pF
$C_{o(tr)}$	Time Related Output Capacitance			372		
$Q_{g(tot)}$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 35\text{ A},$ $V_{GS} = -5\text{ V} / 18\text{ V},$ Inductive load		91		nC
Q_{gs}	Gate to Source Charge			25		
Q_{gd}	Gate to Drain "Miller" Charge			21		
R_G	Internal Gate Resistance	$f = 1\text{ MHz}$		3.0		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 400\text{ V}, I_D = 35\text{ A},$ $V_{GS} = -5\text{ V} / 18\text{ V}, R_G = 5.6\text{ }\Omega,$ FWD : PCH65S20D1, Inductive load		19		ns
t_r	Turn-On Rise Time			17		
$t_{d(off)}$	Turn-Off Delay Time			40		
t_f	Turn-Off Fall Time			8		
E_{on}	Turn-on Switching Energy			65		μJ
E_{off}	Turn-off Switching Energy			105		
E_{tot}	Total Switching Energy			170		

Source-Drain Diode Characteristics

I_S	Maximum Continuous Diode Forward Current			84	A
I_{SM}	Maximum Pulsed Diode Forward Current			225	
V_{SD}	Diode Forward Voltage	$V_{GS} = -5\text{ V}, I_{SD} = 35\text{ A}$		4.2	V
t_{rr}	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 35\text{ A},$ $di_F/dt = 1000\text{ A}/\mu\text{s},$ Includes Q_{OSS}		20	ns
Q_{rr}	Reverse Recovery Charge			141	nC
I_{rrm}	Peak Reverse Recovery Current			11.5	A

Typical Performance Characteristics

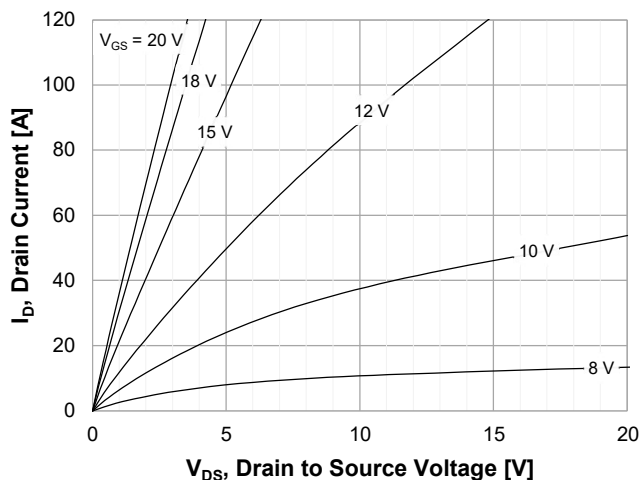
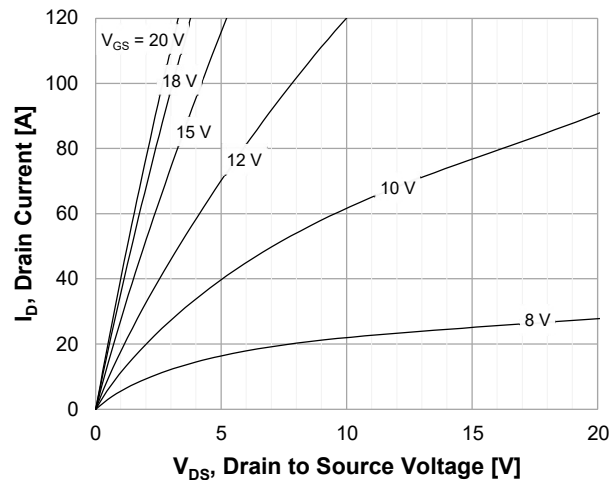
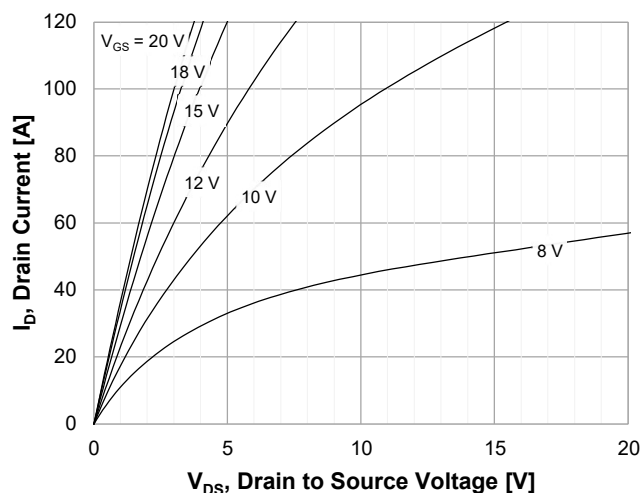
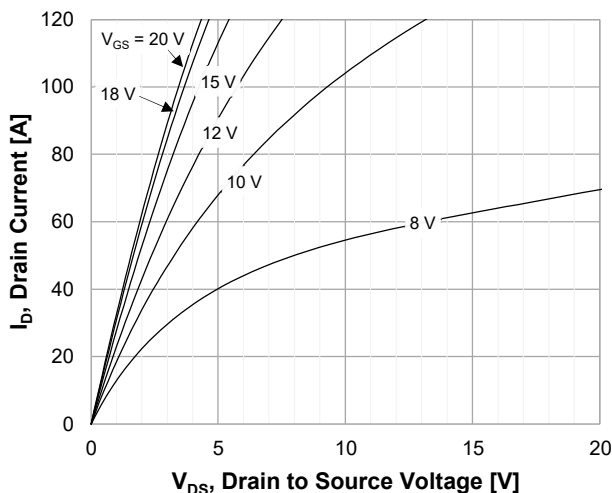
Figure 1. On-Region Characteristics $T_J = -40^\circ\text{C}$ Figure 2. On-Region Characteristics $T_J = 25^\circ\text{C}$ Figure 3. On-Region Characteristics $T_J = 125^\circ\text{C}$ Figure 4. On-Region Characteristics $T_J = 175^\circ\text{C}$ 

Figure 5. On-Resistance Characteristics vs. Temperature

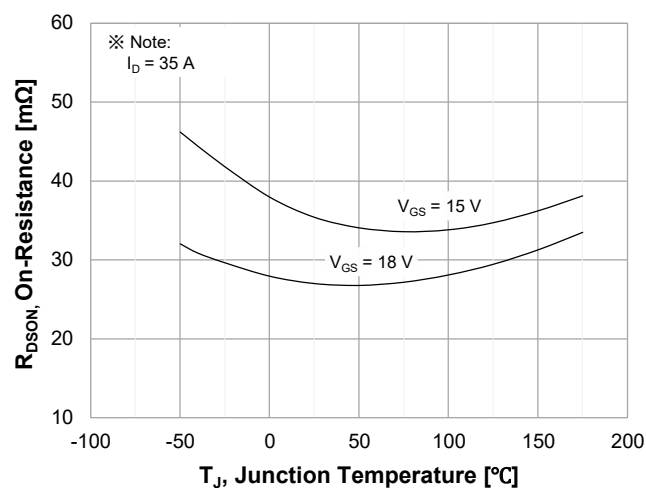
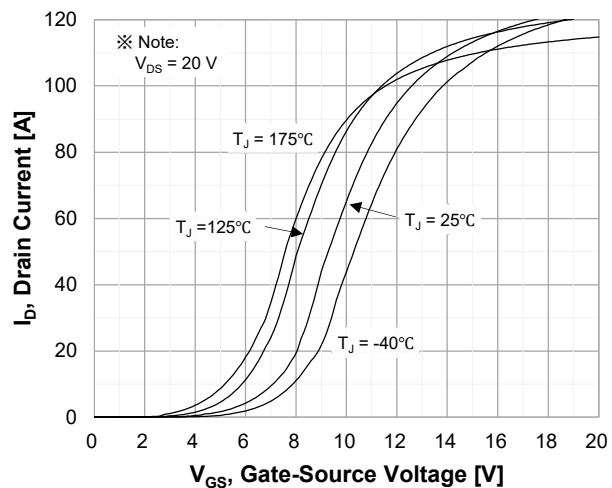


Figure 6. Transfer Characteristics



Typical Performance Characteristics

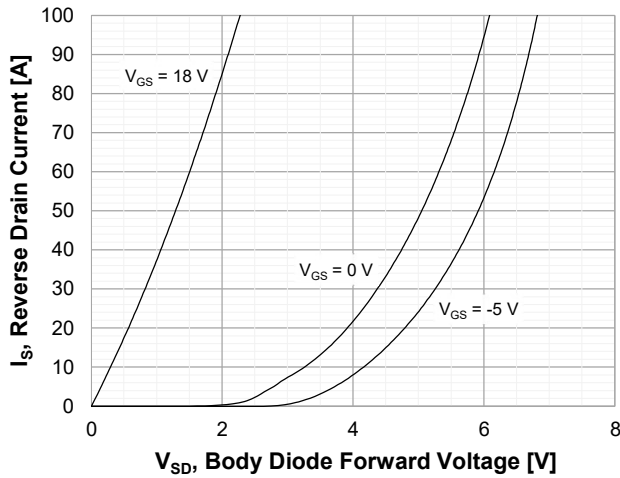
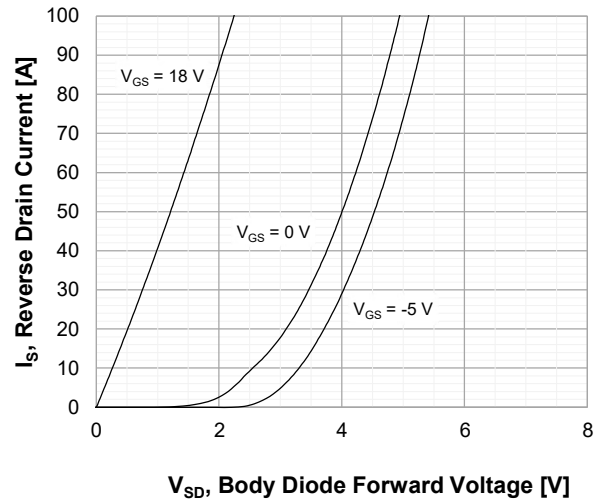
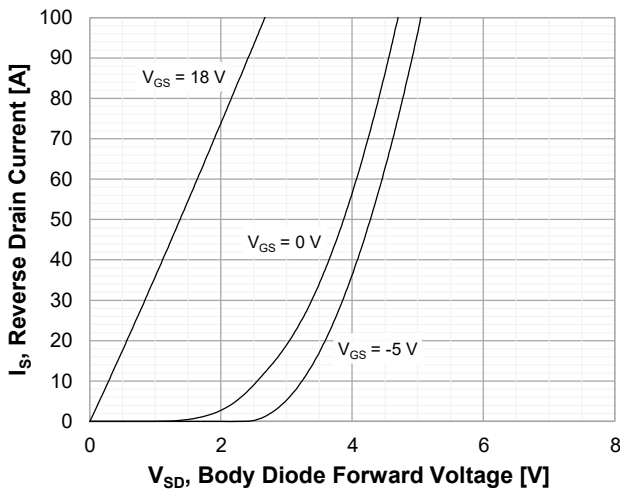
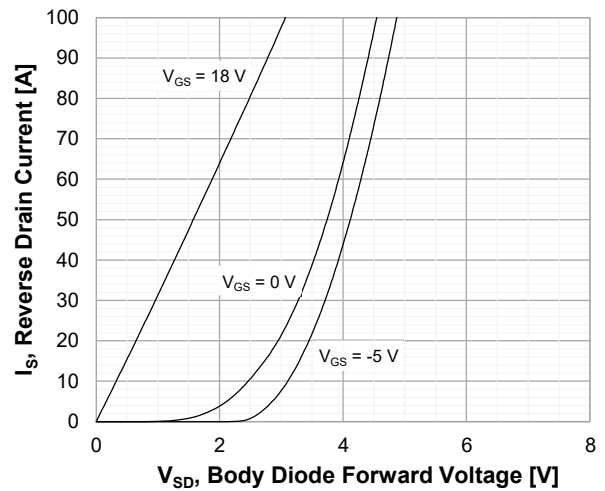
Figure 7. Diode Forward Voltage Characteristics vs. Source-Drain Current $T_J = -40^\circ\text{C}$ Figure 8. Diode Forward Voltage Characteristics vs. Source-Drain Current $T_J = 25^\circ\text{C}$ Figure 9. Diode Forward Voltage Characteristics vs. Source-Drain Current $T_J = 125^\circ\text{C}$ Figure 10. Diode Forward Voltage Characteristics vs. Source-Drain Current $T_J = 175^\circ\text{C}$ 

Figure 11. Threshold Voltage vs. Temperature

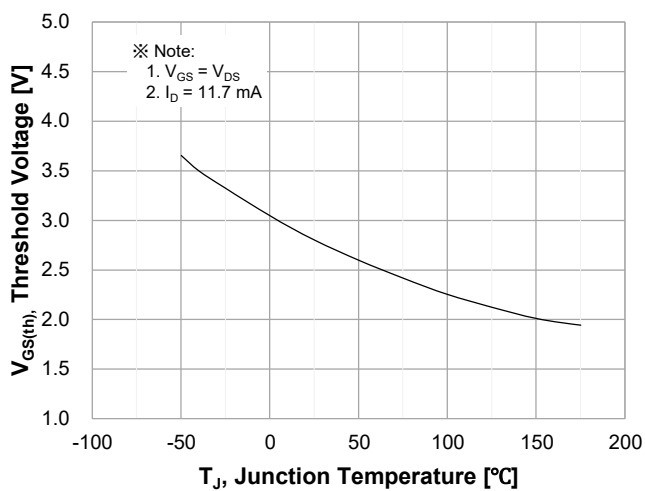
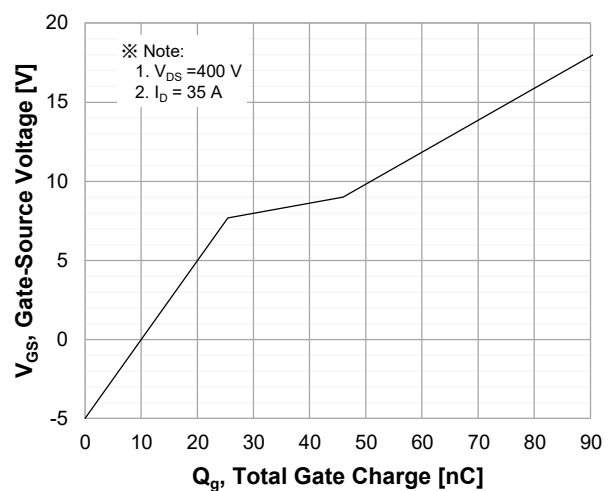


Figure 12. Gate Charge Characteristics



Typical Performance Characteristics

Figure 13. Stored Energy in Output Capacitance

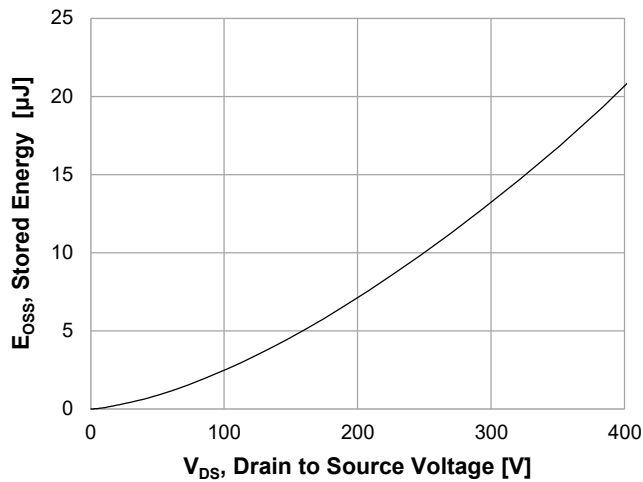


Figure 14. Capacitance Characteristics

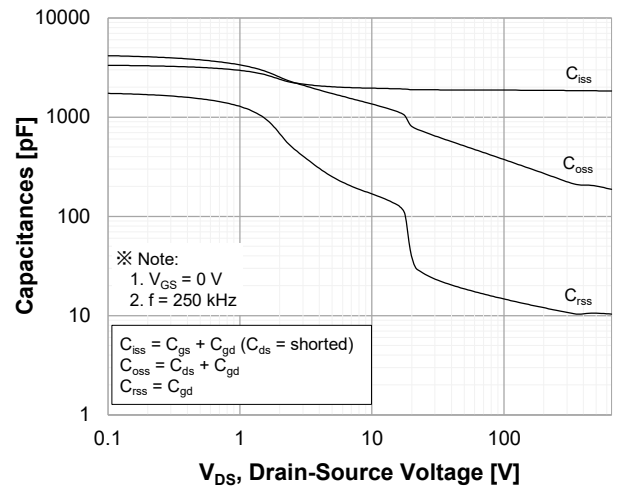


Figure 15. Continuous Drain Current Derating vs. Case Temperature

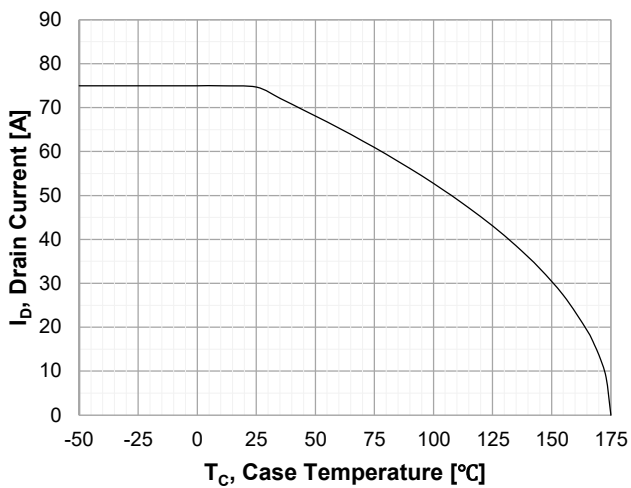


Figure 16. Maximum Power Dissipation Derating vs. Case Temperature

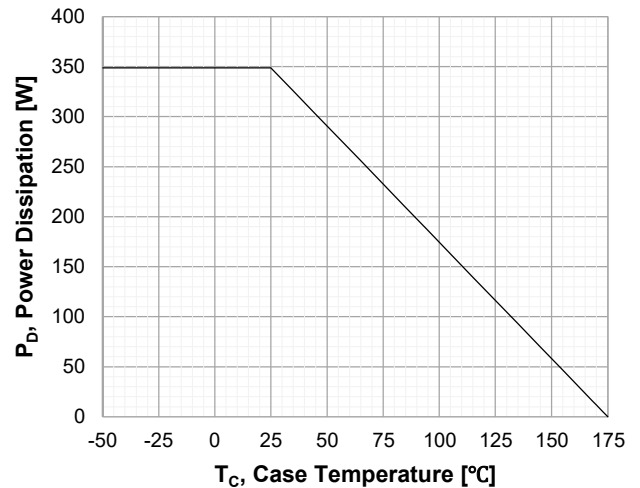


Figure 17. Typ. Switching Losses vs. Drain Current

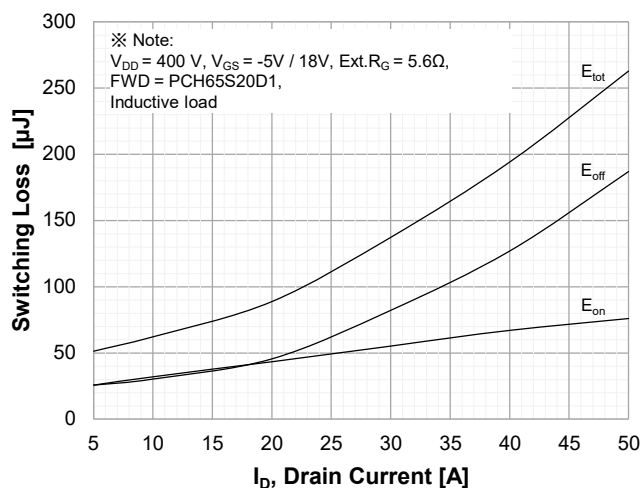
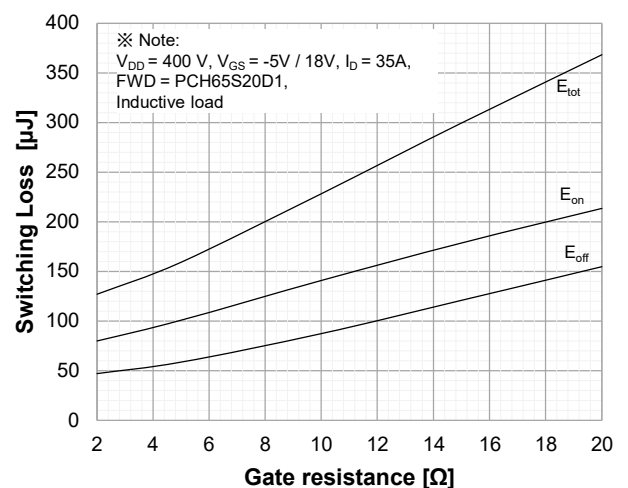


Figure 18. Typ. Switching Losses vs. Gate Resistance



Typical Performance Characteristics

Figure 19. Typ. Switching Losses vs. Drain Current

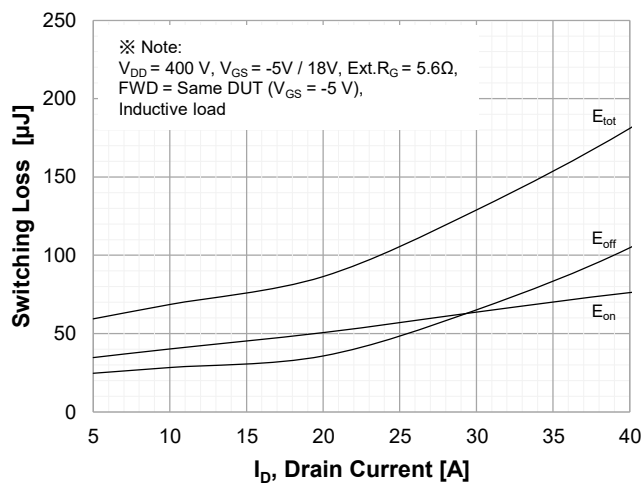


Figure 20. Typ. Switching Losses vs. Gate Resistance

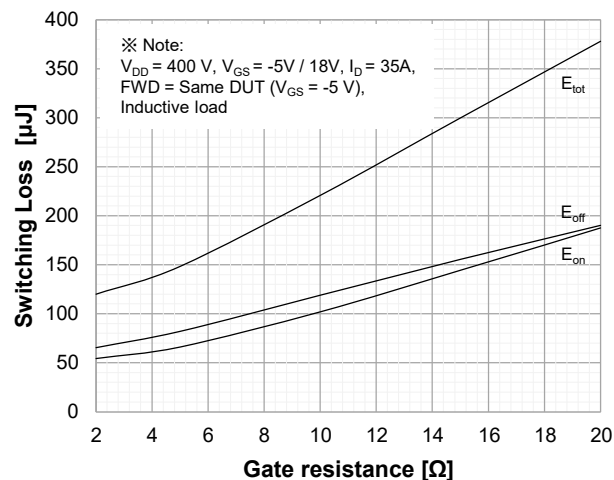


Figure 21. Maximum Safe Operating Area

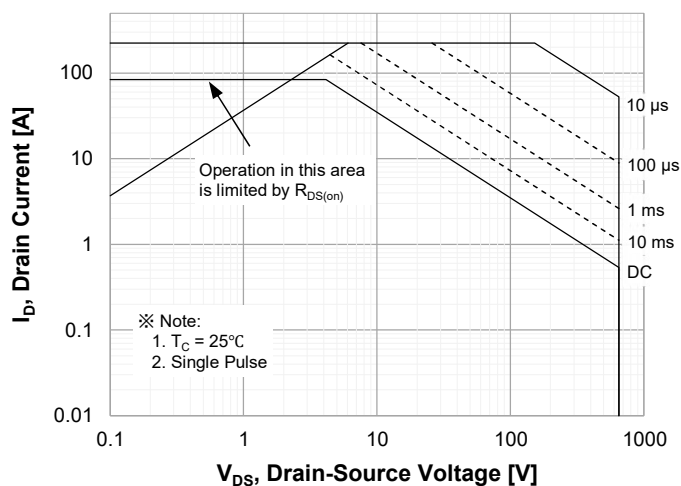
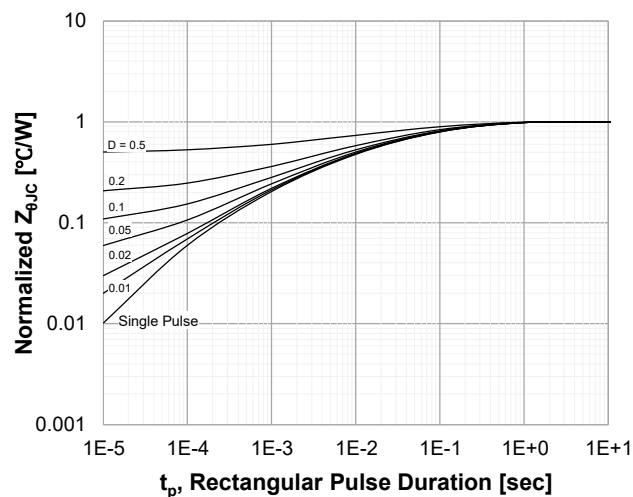


Figure 22. Transient Thermal Response Curve



Typical Performance Characteristics

Figure 23. Inductive Load Switching Test Circuit and Waveforms

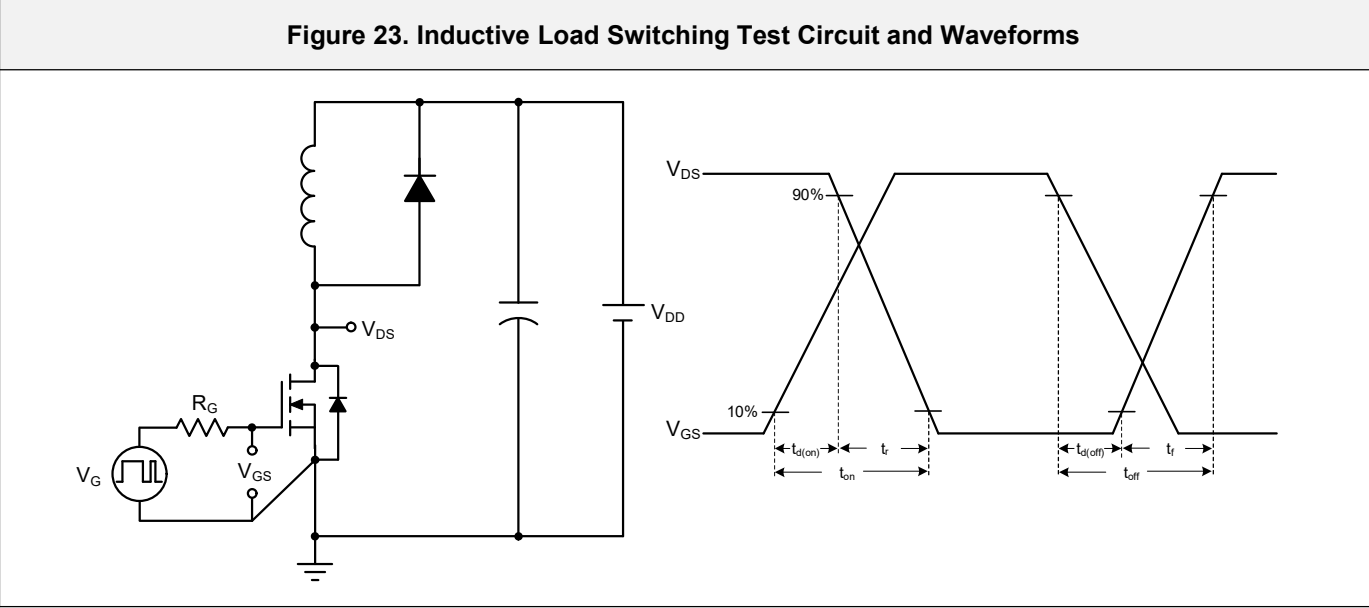
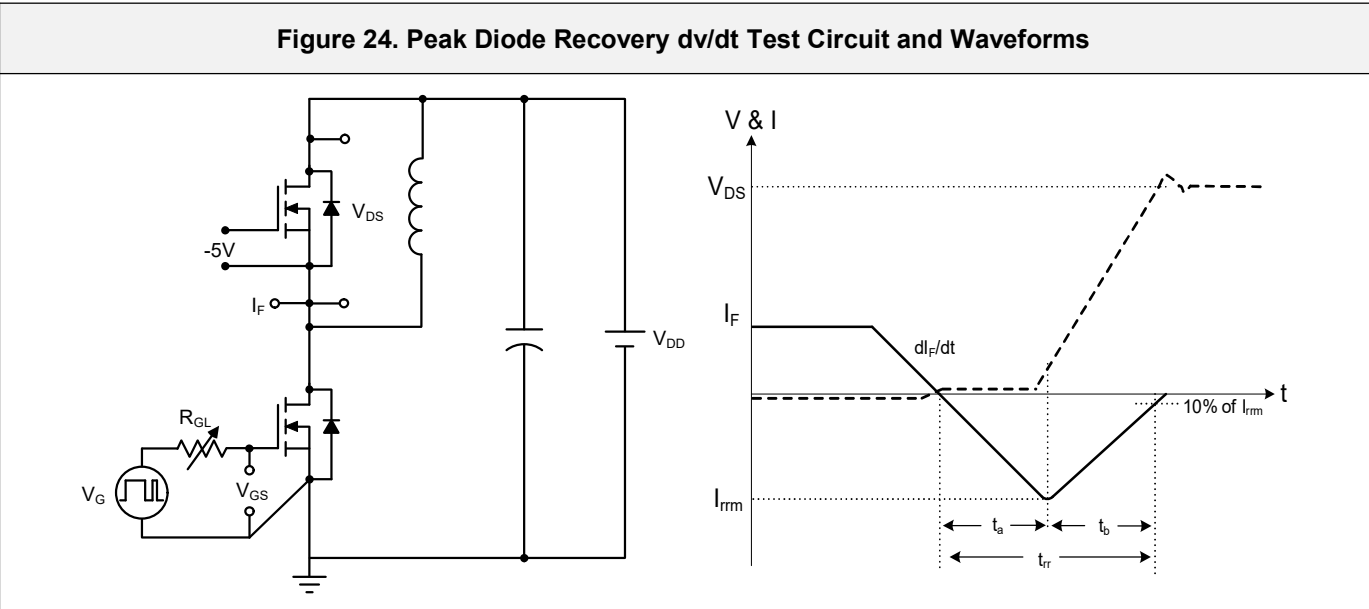
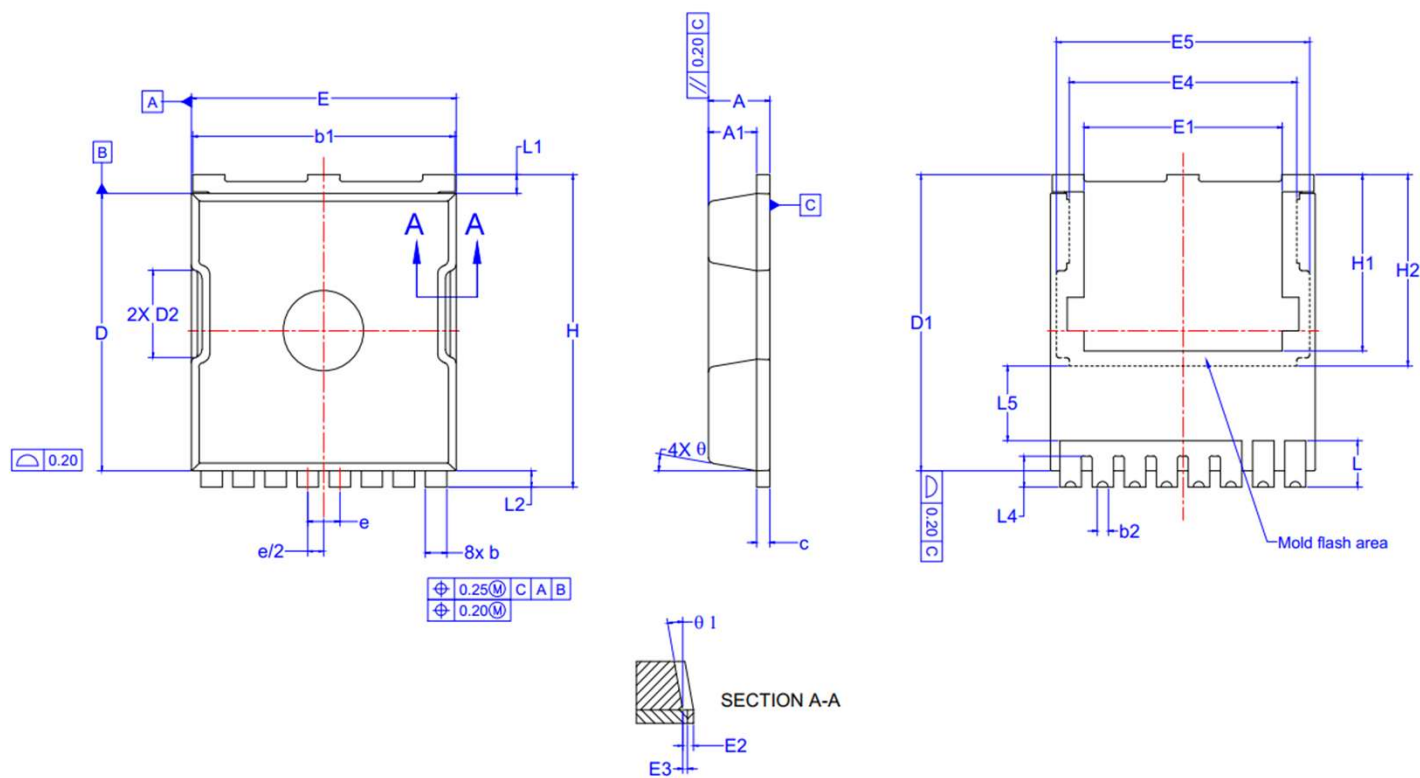


Figure 24. Peak Diode Recovery dv/dt Test Circuit and Waveforms



Package Outlines

TOLL



SYMBOL	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.41	0.51
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.30		
E	9.80	9.90	10.00
E1	7.32	7.42	7.52
E2	0.30	0.40	0.50
E3	0.15	0.18	0.21
E4	8.50		
E5	9.46		
e	1.20 BASIC		
H	11.58	11.68	11.78
H1	6.55	6.65	6.75
H2	7.05	7.15	7.25
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L4	1.00	1.15	1.30
L5	2.70	2.80	2.90
N	8		
θ	10° REF.		
θ1	10° REF.		

* Dimensions in millimeters