

HMF65N380E7

N-Channel MOS E7 Power MOSFET

650 V, 9.6 A, 380 mΩ

Description

The 650V MOS E7 is an advanced Power Master Semiconductor's Super Junction MOSFET family by utilizing charge balance technology for excellent low on-resistance and gate charge.

This technology combines the benefits of an excellent switching performance with ease of usage and robustness.

Consequently, the 650V MOS E7 family is suitable for application requiring superior efficiency and extra safety margin for design with higher voltage.

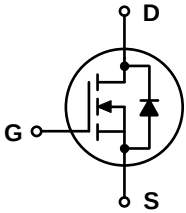
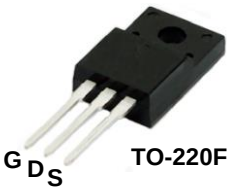
Applications

- PFC, Hard & Soft Switching Topologies
- Industrial & Consumer Power Supplies

Features

$BV_{DSS} @ T_{J,max}$	I_D	$R_{DS(on),max}$	$Q_{g,typ}$
700 V	9.6 A	380 mΩ	16.5 nC

- Reduced Switching & Conduction Losses
- Lower Switching Noise
- 100% Avalanche Tested
- Pb-free, Halogen Free, and RoHS Compliant



Absolute Maximum Ratings ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage		± 30	V
I_D	Drain Current	Continuous ($T_C = 25^{\circ}\text{C}$)	9.6*	A
		Continuous ($T_C = 100^{\circ}\text{C}$)	6.1*	
I_{DM}	Drain Current	Pulsed (Note1)	28.8*	A
E_{AS}	Single Pulsed Avalanche Energy (Note2)		40	mJ
I_{AS}	Avalanche Current (Note2)		2.5	A
E_{AR}	Repetitive Avalanche Energy (Note1)		0.87	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note3)		20	
P_D	Power Dissipation	($T_C = 25^{\circ}\text{C}$)	28	W
		Derate Above 25°C	0.22	W/ $^{\circ}\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	$^{\circ}\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		260	$^{\circ}\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.5	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
HMF65N380E7	HMF65N380E7	TO-220F	Tube	50 units

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	700			
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		2		
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.8\text{ mA}$	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$		318	380	m Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 250\text{ kHz}$		624		pF
C_{oss}	Output Capacitance			17		pF
$C_{o(tr)}$	Time Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		224		pF
$C_{o(er)}$	Energy Related Output Capacitance			28		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400\text{ V}, I_D = 4\text{ A},$ $V_{GS} = 10\text{ V}$		16.5		nC
Q_{gs}	Gate to Source Charge			3.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			8.2		nC
R_G	Gate Resistance	$f = 1\text{ MHz}$		6.9		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 400\text{ V}, I_D = 4\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 10\text{ }\Omega$ See Figure 13		9		ns
t_r	Turn-On Rise Time			9		ns
$t_{d(off)}$	Turn-Off Delay Time			39		ns
t_f	Turn-Off Fall Time			10		ns

Source-Drain Diode Characteristics

I_S	Maximum Continuous Diode Forward Current			9.6	A
I_{SM}	Maximum Pulsed Diode Forward Current			28.8	A
V_{SD}	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 4\text{ A}$		1.2	V
t_{rr}	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 4\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		220	ns
Q_{rr}	Reverse Recovery Charge			1.78	μC

※Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 2.5\text{ A}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 4\text{ A}, di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

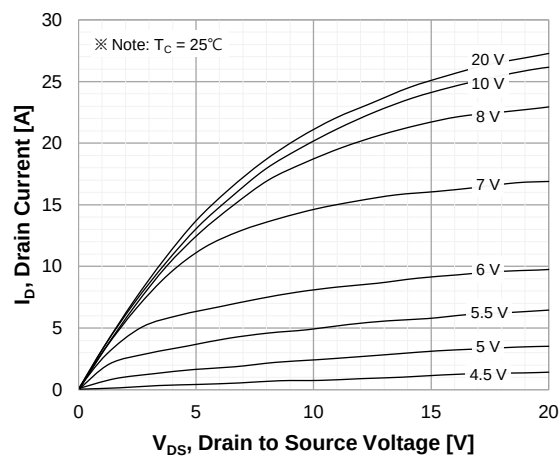


Figure 2. Transfer Characteristics

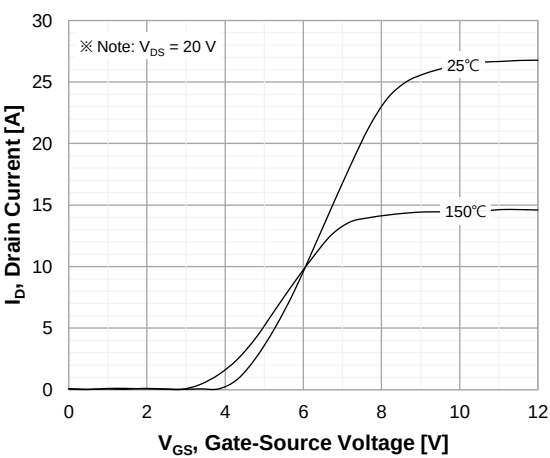


Figure 3. On-Resistance Characteristics vs. Drain Current and Gate Voltage

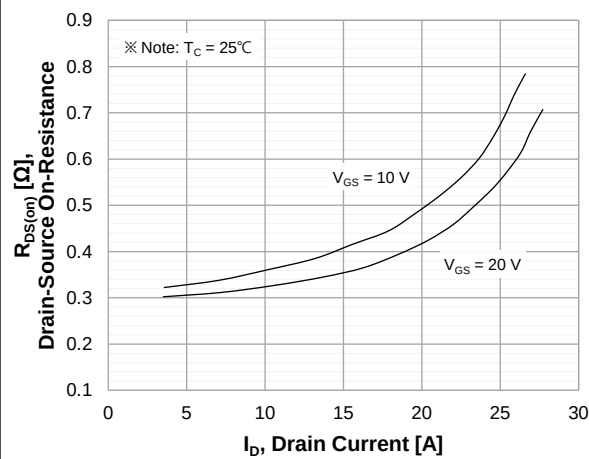


Figure 4. Diode Forward Voltage Characteristics vs. Source-Drain Current and Temperature

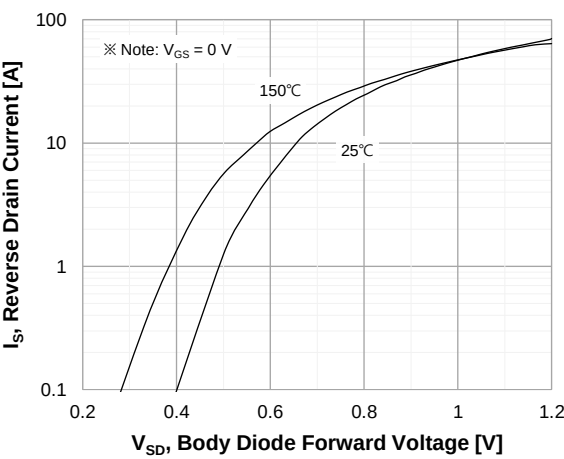


Figure 5. Capacitance Characteristics

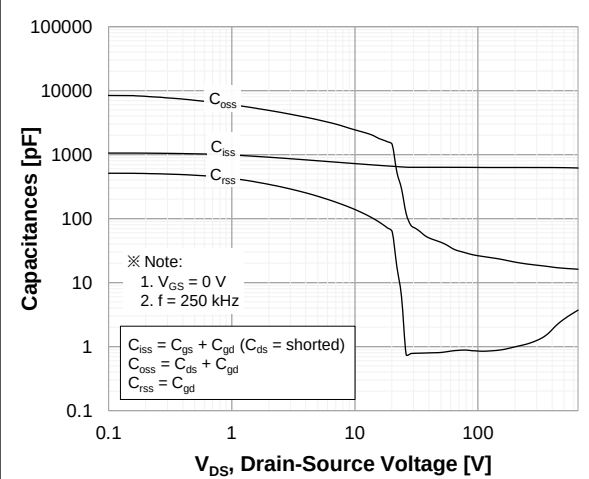
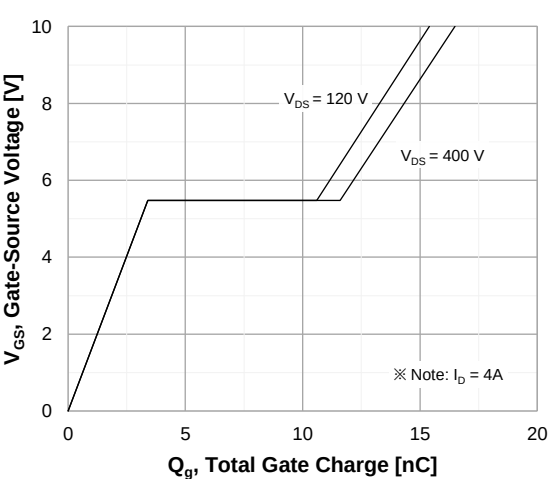


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Characteristics vs. Temperature

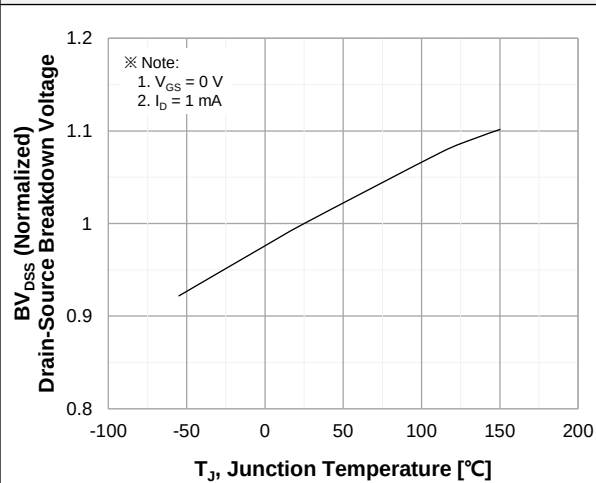


Figure 8. On-Resistance Characteristics vs. Temperature

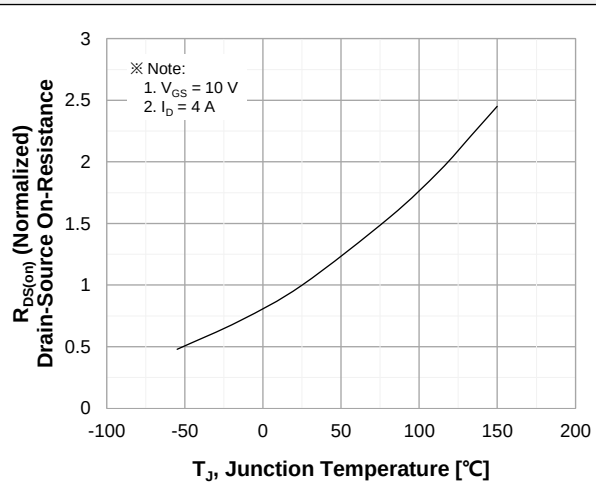


Figure 9. Maximum Safe Operating Area

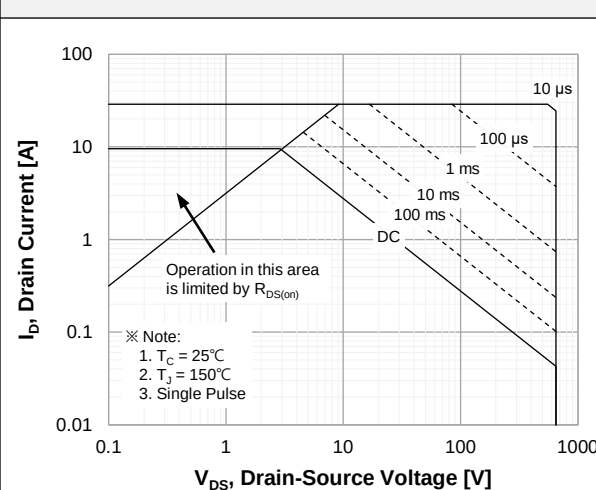


Figure 10. Maximum Drain Current vs. Case Temperature

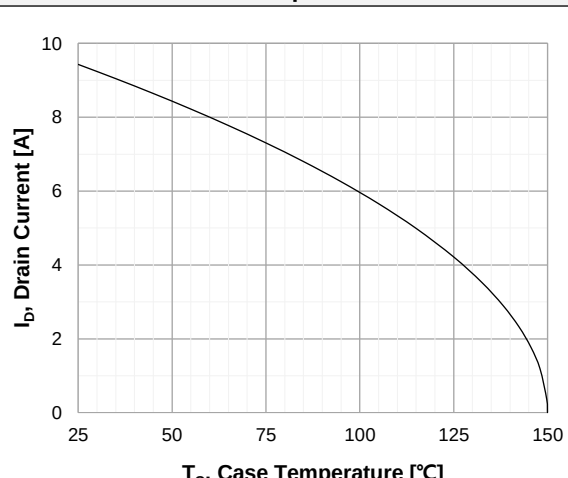


Figure 11. E_{oss} vs. Drain to Source Voltage

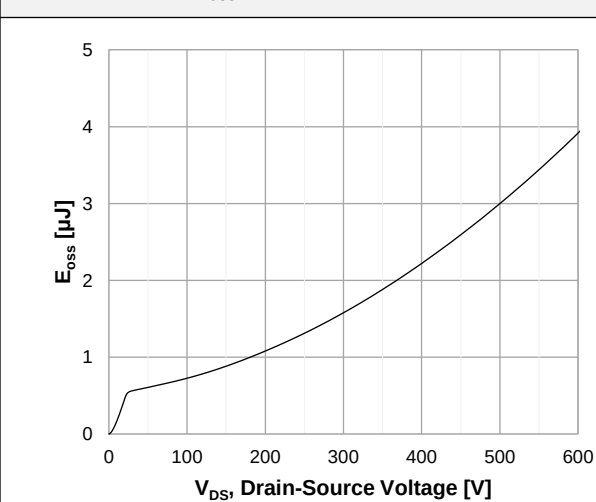
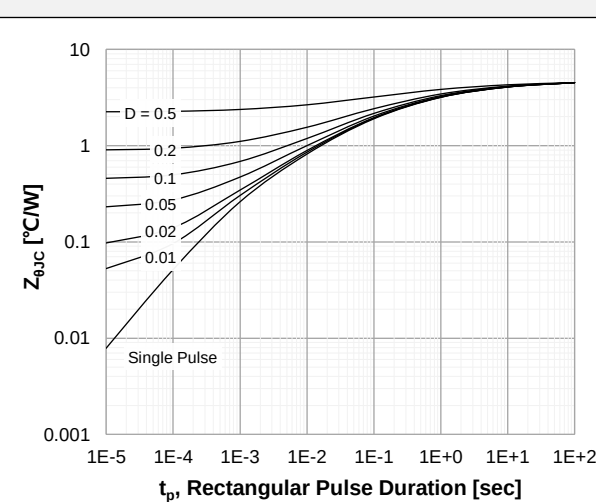


Figure 12. Transient Thermal Response Curve



Test Circuits

Figure 13. Inductive Load Switching Test Circuit and Waveforms

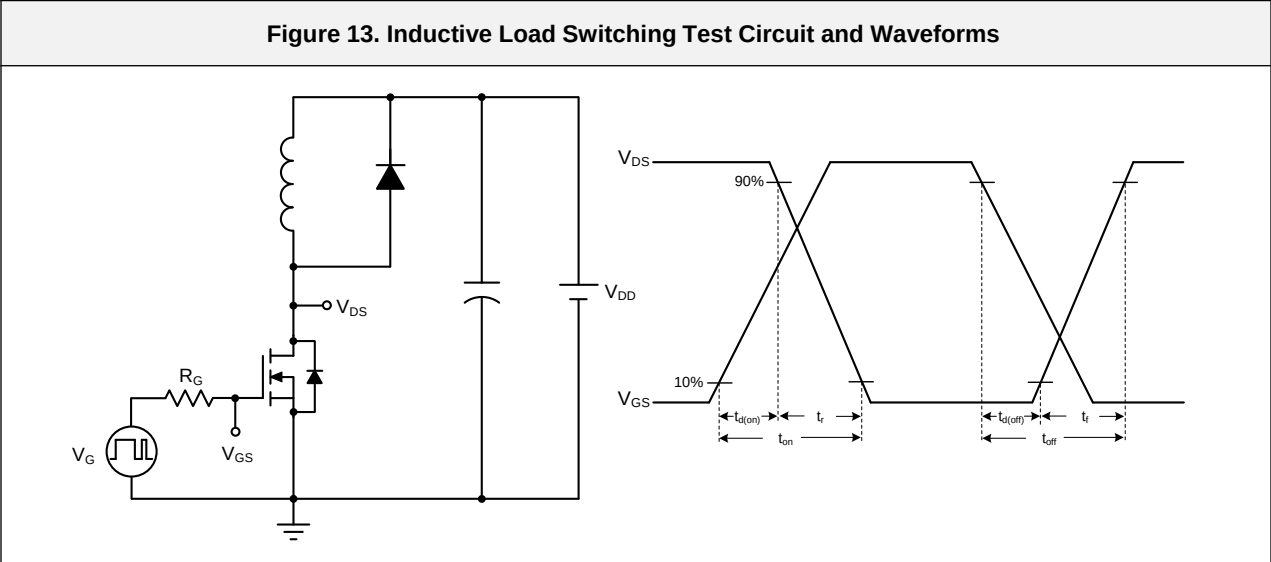


Figure 14. Unclamped Inductive Switching Test Circuit and Waveforms

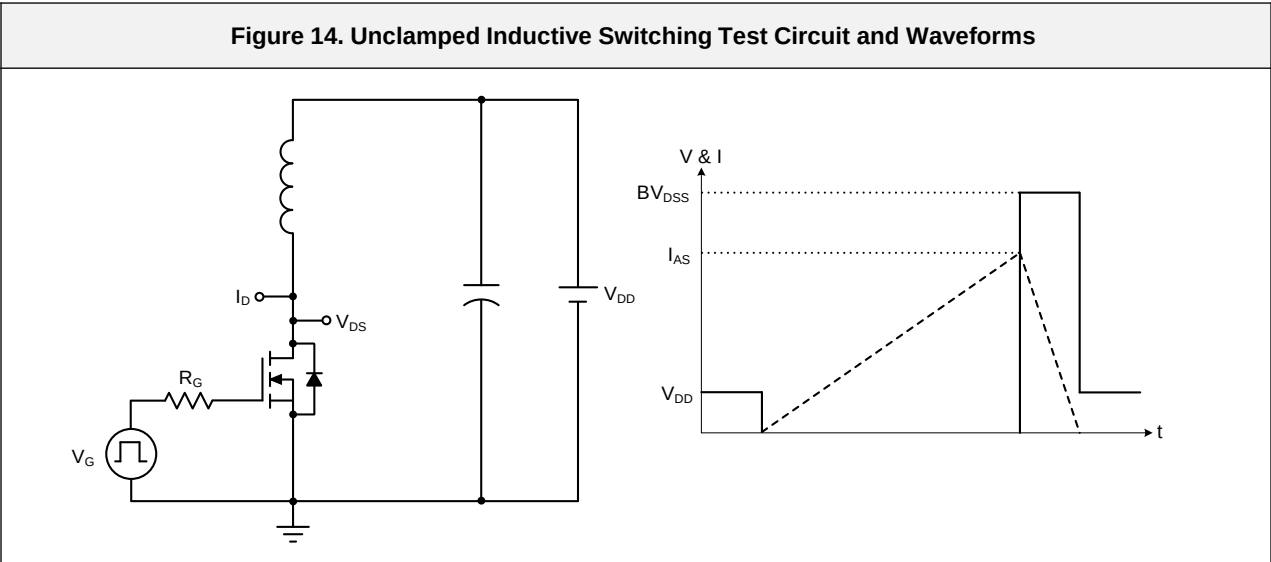
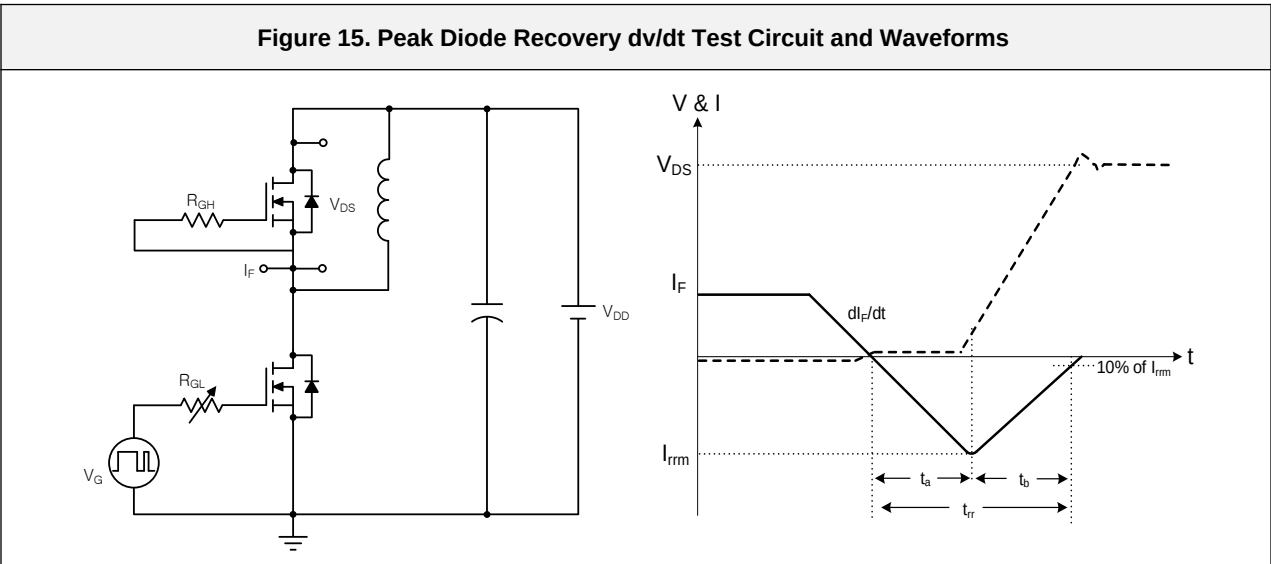
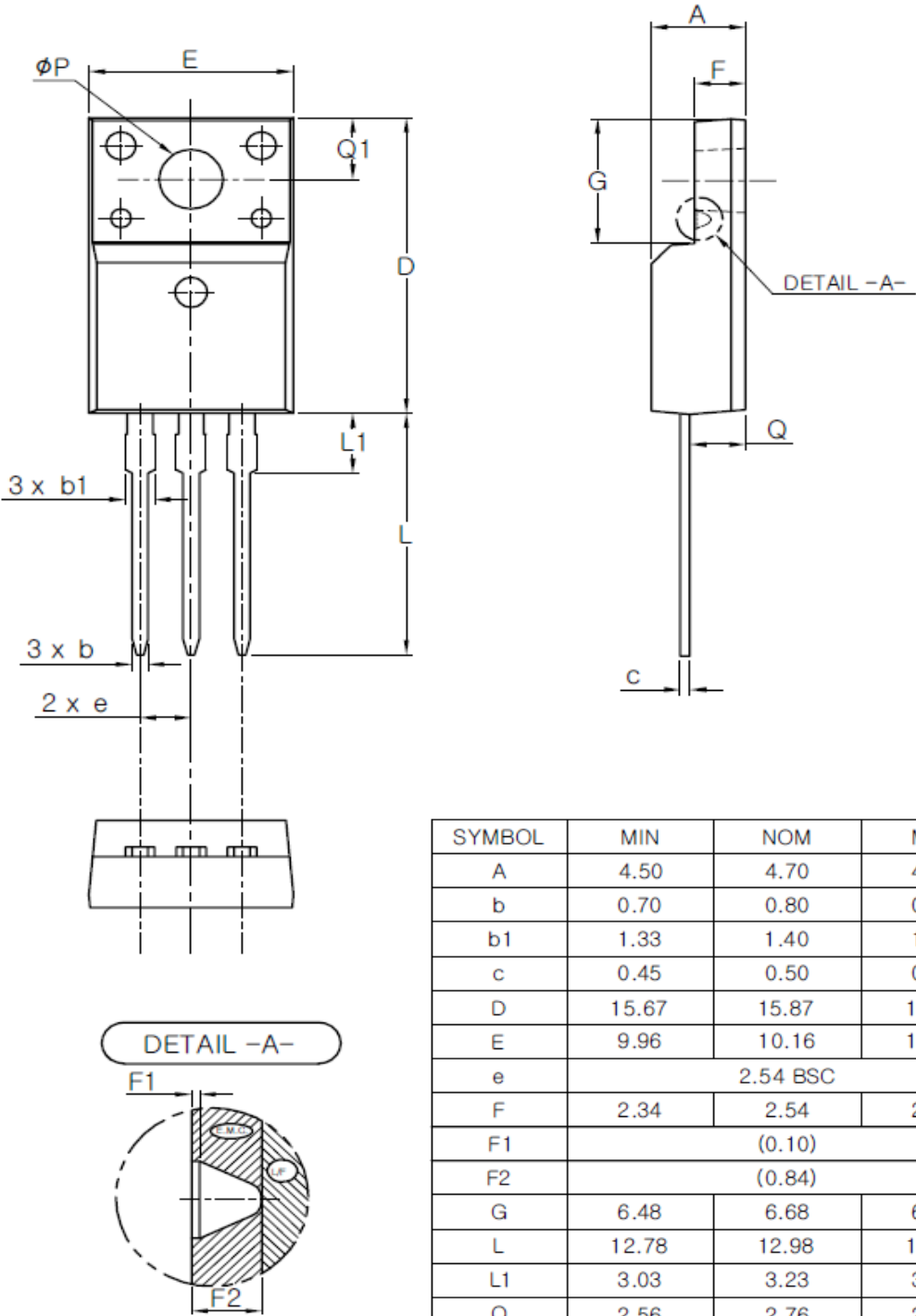


Figure 15. Peak Diode Recovery dv/dt Test Circuit and Waveforms



Package Outlines

TO-220F



SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.90
b	0.70	0.80	0.90
b1	1.33	1.40	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
E	9.96	10.16	10.36
e	2.54 BSC		
F	2.34	2.54	2.74
F1	(0.10)		
F2	(0.84)		
G	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Q	2.56	2.76	2.96
Q1	3.10	3.30	3.50
ϕP	3.08	3.18	3.28

* Dimensions in millimeters